

Contract Information

Contract Number	N00014-03-1-0434
Title of Research	Virtual prototyping, advanced electric systems, and controls for ships
Dates	June 15, 2003 to March 31, 2004
Principal Investigator	Roger A. Dougal
Organization	University of South Carolina

Technical Section

Technical Objectives

The three principal objectives of this work were to -- 1) Advance the capabilities for virtual prototyping of advanced electric systems with emphasis on: simulation of uncertain systems, tools for rapid model development, realtime and distributed simulation with hardware in the simulation loop including enforcement of natural coupling laws at the interface points between the real and virtual components of the system, and security of the simulation environment. 2) Develop new control methods and algorithms and new methods for rapid prototyping and insertion of controls into power electronic systems, with emphasis on manifold-based control schemes especially as applied to local systems of competing loads, and the man-machine interface for controls. And 3) develop new understandings of the stability and dynamic performance of emerging shipboard power system architectures and new methods for characterizing the risk, stability, and performance of those systems.

Technical Approach

Objective 1: Virtual Prototyping

The Virtual Test Bed software was used as the framework for developing, testing, and proving out new concepts in system simulation. As new capabilities were developed they were merged into the release version of the software so that they became available to the greater user community. This work was performed in conjunction with Univ of Arkansas (Alan Mantooth), Taganrog University (Vadim Popov et. al and V. Gusik et. al), and Interactive Data Visualization (Chris King, et. al).

A significant focus of this work was on developing a version of VTB that runs under Linux, which provides better real-time support than does MS Windows. Three hardware environments for this system were used -- 1) a cluster of single-processor Linux computers, 2) a multiprocessor (four 64-bit Itanium processors) computer with shared memory, and 3) multiple independent single-processor cards installed in an industry-standard (expandable) VXI-bus crate.

Objective 2: New control methods

Manifold-based control methods such as sliding mode, synergetic, and immersion and invariance were developed and applied to power electronic systems. This work was performed in collaboration with colleagues at Northeastern university (Alex Stankovic, et. al) and Taganrog University (Anatoly Kolesnikov, et. al). Tools to automate the design of synergetic controllers were developed.

Methods for rapid control development, validation, and insertion were built on the capabilities of the VTB such as the dynamic interface to Simulink, and on the capabilities of other commercial hardware such as the dSpace system for rapid testing of digital controls. The tight linking of these two

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environments guarantees a seamless integration of the control design and testing process. Additional methods for testing controls running on embedded processors while in the VTB simulation loop provide the last stage of control validation.

Objective 3: Power System architectures and performance

Simulation models of new power system architectures were used to study the dynamic performance of those systems. For example, one study examined the relative performance of multiple-generator systems when the inter-generator coupling is via a DC link as compared to an AC link.

Other efforts sought to develop methods for defining system stability and risk indices, based on time-domain measurements of the system response, but applying frequency domain and wavelet-based analysis techniques. Innovative techniques were required because of the multi-language capabilities of the VTB – one cannot be certain that every model contains methods for every type of analysis that one might desire to perform.

As preliminaries to some of these analyses, models of various power system components were developed.

Progress

Objective 1: Virtual Prototyping

Significant progress was made in three areas

- VTB Realtime running under Linux
- Methods for user creation of new models
- Methods for simulation of uncertain systems

The VTB solver called “resistive companion with signal extensions” was successfully ported to Linux and executed under realtime protocols. The solver was tested on several configurations of computing hardware, including single processor workstation, multiprocessor workstation, and a VXI-bus based multiprocessor system that is compatible with industrial automation systems. The Linux/RealTime version of VTB supports hardware in the simulation loop via standard data I/O cards from e.g. National Instruments, using shareware hardware drivers supplied by the Linux Control and Measurement Device Interface (Comedi) project.

Several methods for user-creation of new models were developed. New capabilities were inserted into the existing User Defined Device (UDD) object to allow it to take full advantage of the capabilities of VTB2003, including support for multi-layer icons, matrix ports, and conditional statements. There are two versions of the UDD – one that generates a resistive companion model during VTB run-time, and a second that generates C++ code for subsequent compilation and production of a standard VTB model (vtm file). This code can be compiled by any C++ compiler.

The study of interactions between model order and time step has produced specific algorithms for adjusting time step and model order for one test case. The test case was not globally representative of all cases, so there is still much to be learned about this simulation mode. Nonetheless, the study did produce a quantitative comparison of the execution time and accuracy of the test case against fixed model order and fixed time step cases. In a particular test case involving a hybrid battery/capacitor energy storage device, a speed improvement of more than 50% was achieved, while maintaining simulation accuracy within 0.7%.

A stepping API was developed for the VTB solver. This expands the utility of VTB in two ways. First, it allows the solver engine to recursively call instances of itself. This capability allows complex system models to be broken into faster-executing sub-system models that can execute on (optionally)

independent machines. Secondly, it allows the VTB solver to be called by other applications. This makes the relationship between VTB and those other applications (e.g. Matlab) symmetrical rather than one-sided; either application can call the other.

Active X techniques for data sharing or cosimulation within VTB have now been developed for Matlab/Simulink and are next being developed for Labview. This approach is Windows specific, so will not be employed in the RT version (under Linux), but is expected to enhance the functionality, capabilities, and speed of VTB on Windows machines.

A program that generates a histogram of the frequency of the import call-functions for all VTB models was developed with the aim of using the histogram to detect patterns of calls that could identify malicious code. This is a preliminary step in implementing an automatic tool for model security.

Code generation from Paragon. The XML/MathML-based database of Paragon was redesigned and enhanced by adding formal analysis methods of model data represented in the XML schema. Paragon builds an Abstract Syntax Tree (AST) from the XML schema, which is used to represent all the information of the model in a specific format suitable for rigorous analysis. For the purpose of code generation for VTB2002/3 (as well as other HDLs such as VHDL-AMS and Mast) modules/methods have been written which extract and analyze all the information from AST. A first integration of the User Defined Device/Paragon/Universal Translator technologies of USC, Univ. Ark, and Taganrog University was accomplished. Enhancements to the runtime version of the UDD tool now provide the capability to handle signal type ports. The new version of UDD supports multilayer icons, up to 5 inputs/outputs or an unlimited number of inputs/outputs via matrix ports.

An L/U type sparse matrix solver method has been developed to replace the existing conjugate-gradient sparse method that is currently used in the VTB solver. The L/U method avoids certain types of convergence failures because it is not an iterative method. The method has been tested on several systems and shows an approximately linear increase in speed-up with increase in system complexity, compared to non-sparse methods.

A new version of the uncertainty solver based on Polynomial Chaos Theory was created. The new solver encapsulates existing (classical) VTB models within a new framework, thereby vastly expanding the range of systems that can be described as uncertain systems. (Because now models of well-characterized components do not need to be reformulated to operate with the uncertainty solver). Also, this allows a user to progressively remove uncertainty from a system by using the deterministic models as items become certain. The new solver is running now, but will be tested intensively before being released. This solver dramatically changes the methods of simulating partially unknown systems - which have been traditionally involved monte carlo approaches that incorporate a large number of simulation runs. Now, a single run, can yield copious information about the probabilistic distribution of the end result or can analyze sensitivity to parameters.

Use of Semantic Web techniques and tools to search for VTB models was completed. The Semantic Web aims to encode semantics into web documents so that machines can meaningfully manipulate the data they contain. Based on those techniques, we have developed a system that uses concepts and tools from the Semantic Web to enable intelligent searching for models in a system prototyping environment. We determine the semantic-distance between objects from our domain and queries. This distance is used to determine the best match for a query. To determine the semantic-distance we use an instance based learning method, specifically a K-Nearest neighbor approach is used. We place both the model and the query in N-dimensional space and compute the distance. To place the models in N-dimensional space we utilize a rule-engine that applies rules based on the semantics of an ontology language and rules specific

to our domain. These rules add additional information to our knowledge base beyond that which can be extracted from the models. This additional information makes a more intelligent search possible. The extension of this research now begins to develop an Agent-Interface to the schematic editor. The first test of the agent interface will entail remote execution of schematic editor events, such as parameter changes and entity additions. We anticipate that the agent interface will lead to development of assisted design methods that utilize multi agent systems techniques.

An application of *processor in the loop* simulation with multitasking of the processor was demonstrated, showing that VTB can handle the complexities of time stepping and event seeking in that situation. Software was developed to support the multiple serial port interface for VTB according to a master/slave protocol for communication. The master polls the slave nodes in sequence and waits for responses. Code was written using Win32 API functions to send and receive data and toggle the RTS line. Sending and receiving are overlapped on separate threads, which allows other work to be performed while the I/O operation is pending. This will support incorporation of hardware digital systems into the virtual prototype of a system.

Support for hardware in the loop was enhanced by development of a new hardware interface based on a field programmable gate array (FPGA). The new interface allows very high time resolution for the hardware switching circuits (e.g. PEBBs) while still allowing relatively long time steps in the virtual components of the system so as to preserve high computing speed. The interface is based on a high performance Virtex II Pro (XC2VP4) Xilinx FPGA, which allows to integrate the switching gate control signal, coming from the hardware digital controller, with very high time resolution. The XC2VP4 development board from Memec Design features a 100MHz clock, which yields up to 10ns time resolution. The ISE software from Xilinx is used as the development environment, and is integrated with Matlab for a faster design process.

New models of essential electronic power system components were developed, including models of IGBTs operating at cryogenic temperatures, and detailed models of IGBTs and IGCTs.

Objective 2: New control methods

Control methods based on recurrent wavelet neural networks were tested on the task of identifying the speed of a DC motor without any direct speed sensors in order to implement a motor speed control. The recurrent wavelet neural network (RWNN) was first trained in Matlab and then the RWNN-based speed estimator model was constructed in VTB based on the well trained RWNN. The network structure was determined according to the DC motor dynamic equations, and then the recurrent WNN was trained using the Back Propagation approach. A virtual prototype of the WNN speed estimator was constructed in VTB using the hierarchical modeling approach and existing base models. The model is composed of an input layer, a wavelet activation layer and an output layer. The input layer contains three signal ports for the voltage input, the prior one-step-delay speed input, and the two-step-delay speed input. The wavelet activation layer contains 10 activation daughter wavelets "MWs", a bias input vector and the network-input weight factors. The output layer includes the network-output weights. The speed estimator has not yet been tested; results will be reported next month. Such RWNN estimators may ultimately have many uses in shipboard power systems, not only for motor control but also for estimation of the parameters of the immediate network configuration in reconfigurable power networks.

The tool for automatic generation of control laws based on synergetic control theory was successfully tested for a non-linear system composed of a brushless motor. A new control was developed, introducing an original macrovariable definition, and the control was synthesized using the automatic tool. A preliminary simulation test confirmed the good performance of the control. Two approaches were

considered for estimation of coefficients of the synergetic control laws for power sharing between multiple dc-dc converters. Simulation based methods and analytical transformation methods were considered. The simulation approach allows for faster tune up of control law coefficients.

The multi-RS232 port interface to VTB, which is needed for control studies with Cartes at FSU was developed. This will provide 10 ports into VTB via the RS-232 protocol.

The applications of synergetic control laws to hierarchical assemblies of dc-dc power converters were studied. The studies included parallel and series connections, and democratic and master-slave approaches to current sharing.

Objective 3: Power System architectures and performance

A simulation model of a permanent magnet exciter for an AC generator (alternator) was developed in order to study the the performance and potential limitations of that exciter vis-à-vis a traditional exciter in an isolated two-generator power system (such as a ship power system). The model was developed in Simulink and inserted into VTB using the simulink-to-vtb tool. The exciter model improves the capability to more accurately simulate power system transient behavior. It provides fast voltage regulation and the parameters can be easily changed to suit different generators or to achieve specific performance characteristics.

The performance of an AC power system supplied by a synchronous generator and subjected to impulse loads was studied.

Publications

Proceedings

- "Modeling and Simulation of a Ship's Power Distribution System," E. Solodovnik, R. Dougal, Z. Wu, proceedings of the Advanced Naval Propulsion Symposium 2004, Herndon, VA, November 2004.
- "Simulation Environment for Performance Assessment of Reconfiguration Controls in Zonal Systems," E. Solodovnik, R. Dougal, A. Monti, proceedings of the Advanced Naval Propulsion Symposium 2004, Herndon, VA, November 2004.
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- "Implementation and Validation of a Physics-based Circuit Model for IGCT with Full Temperature Dependencies," X. Wang, A. Caiafa, J. L. Hudins, E. Santi, P.R. Palmer, proceedings of the 2004 IEEE Power Electronics Specialist Conference, pp. 597-603, June 2004.
- "Synergetic Control for DC-Dc Buck Converters with Constant Power Load," I. Kondratiev, R. Dougal, E. Santi, G. Veselov, proceedings of the 2004 IEEE Power Electronics Specialist Conference, pp. 3758-3764, June 2004.
- "Testing of Digital Controllers Using Real-Time Hardware in the Loop Simulation," X. Wu, H. Figueroa, A. Monti, proceedings of the 2004 IEEE Power Electronics Specialist Conference, pp. 3622-3627, June 2004.
- "Synergetic Control form Parallel-Connected DC-DC Buck Converters," I. Kondratiev, R. Dougal, E. Santi, G. Veselov, proceedings of the 2004 IEEE Power Electronics Specialist Conference, pp. 182-183, June 2004.

Journals

- Temperature Effects on Trench-gate Punch-through IGBTs, *IEEE Transactions on Industry Applications*, Vol. 40, No. 2, pp. 472-482, March/April 2004.

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